

We claim:

- 1 1. An apparatus, comprising:
 2 a table containing a plurality of entries, each entry including a frequency field
 3 and a voltage field; and
 4 a register coupled to the table and having a selection field to select one of the
 5 plurality of entries.
- 1 2. The apparatus of claim 1, wherein the register also has a limit field to specify
 2 how many entries are selectable.
- 1 3. The apparatus of claim 2, wherein the selection field is a read-write field and
 2 the limit field is a read-only field.
- 1 4. The apparatus of claim 1, wherein the frequency field includes a processor
 2 clock frequency indicator.
- 1 5. The apparatus of claim 4, wherein the processor clock frequency indicator is a
 2 multiplier to be used with a phase locked loop circuit to generate a processor clock
 3 frequency.
- 1 6. The apparatus of claim 1, wherein the voltage field includes a processor
 2 operating voltage identifier.

1 7. The apparatus of claim 1, wherein the table is disposed in non-volatile memory.

1 8. The apparatus of claim 7, wherein the table includes at least two entries.

1 9. A computer system, comprising:

2 a clock generator to selectively output a clock signal at any of a plurality of
3 selectable processor clock frequencies;

4 a power supply to selectively output any of a plurality of selectable processor
5 operating voltages;

6 a table coupled to the clock generator and the power supply and containing a
7 plurality of entries, each entry including a frequency field and a voltage
8 field; and

9 a register coupled to the table and having a selection field to select one of the
10 plurality of entries.

1 10. The system of claim 9, wherein the register also has a limit field to specify how
2 many entries are selectable.

1 11 The system of claim 10, wherein the selection field is a read-write field and the
2 limit field is a read-only field.

1 12. The system of claim 9, wherein the frequency field includes a processor clock
2 frequency indicator.

1 13. The system of claim 12, wherein the processor clock frequency indicator is a
2 multiplier to be used with a phase locked loop circuit to generate the processor clock
3 frequency.

1 14. The system of claim 9, wherein the voltage field includes a processor operating
2 voltage identifier.

1 15. The system of claim 9, wherein the table is disposed in non-volatile memory.

1 16. The system of claim 15, wherein the table includes at least two entries.

1 17. A method, comprising:
2 writing into a selection field of a register;
3 using a content of the selection field to select one of a plurality of entries in a
4 table, each entry having a frequency field and a voltage field.

1 18. The method of claim 17, wherein a content of the frequency field indicates a
2 processor clock frequency.

1 19. The method of claim 17, wherein a content of the voltage field identifies a
2 processor operating voltage.

1 20. The method of claim 17, further comprising:
2 using a content of a limit field in the register to determine how many entries are
3 in the plurality of entries.

1 21. The method of claim 17, further comprising:
2 using a content of the frequency field of the selected one of the plurality of
3 entries to control an operating frequency of a processor clock.

1 22. The method of claim 21, wherein using includes using the content of the
2 frequency field as a multiplier to control an output frequency of a phase locked loop.

1 23. The method of claim 17, further comprising:
2 using a content of the voltage field of the selected one of the plurality of entries
3 to control an operating voltage to a processor.

1 24. The method of claim 23, wherein using includes using the content of the voltage
2 field to select from a plurality of operating voltages to the processor.

1 25. The method of claim 17, wherein a content of the frequency field and a content
2 of the voltage field in a selected entry of the table are matched to produce a
3 combination of processor clock frequency and processor operating voltage that are
4 operable in an associated processor.

1 26. A machine-readable medium having stored thereon instructions, which when
2 executed by a processor cause said processor to perform:
3 determining a desired combination of processor clock frequency and processor
4 operating voltage; and

5 writing to a register to select the desired combination of processor clock
6 frequency and processor operating voltage from a table.

1 27. The medium of claim 26, further comprising:
2 reading from the register to determine the current combination of processor
3 clock frequency and processor operating voltage.

1 28. The medium of claim 26, further comprising:
2 reading from the register to determine how many combinations of processor
3 clock frequency and processor operating voltage are available to be
4 selected.

1 29. The medium of claim 26, wherein:
2 determining a desired combination is based on at least one of:
3 a performance goal;
4 a power consumption goal; and
5 operating characteristics of the processor.

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